What is claimed is:

1. An operational amplifier having a differential amplifier stage for performing amplification in response to a difference between a pair of input signals input thereto via a noninverting input terminal and an inverting input terminal respectively, wherein said differential amplifier stage comprises a first constant current source for use in current limitation,

a pair of first MOS transistors, sources of which are commonly connected with a first voltage supply via the first constant current source, and gates of which receive the pair of input signals respectively;

a pair of second MOS transistors of a high voltage resistant type having a same conduction type that is identical to a conduction type of the pair of first MOS transistors, wherein the second MOS transistors are respectively arranged on current paths connecting between drains of the first MOS transistors and a second voltage supply;

a pair of load circuits that are arranged on current paths connecting between drains of the second MOS transistors and the second voltage supply; and

a bias circuit for biasing gates of the second MOS transistors at a prescribed voltage.

2. An operational amplifier according to claim 1, wherein the bias circuit comprises a third MOS transistor in which a source is connected with the first voltage supply via the first constant current source and in which a gate and a source are connected together, a fourth MOS transistor of a high voltage resistant type in which a source is connected with the drain of the third MOS transistor and in which a gate and

a drain are commonly connected with the gates of the second MOS transistors, and a second constant current source that is connected between the drain of the fourth MOS transistor and the second voltage supply.

3. An operational amplifier according to claim 2, wherein current values of the first and second constant current sources are set such that a source-gate voltage of each of the second to fourth MOS transistors is substantially identical to a prescribed gate threshold voltage.

4. An operational amplifier according to claim 2, wherein the first voltage supply produces a positive voltage while the second voltage supply produces a negative voltage, and wherein the first to fourth MOS transistors are all configured as P-channel MOS transistors.

5. An operational amplifier according to claim 3, wherein the first voltage supply produces a positive voltage while the second voltage supply produces a negative voltage, and wherein the first to fourth MOS transistors are all configured as P-channel MOS transistors.

6. An operational amplifier according to claim 1, wherein a first gate threshold voltage is set to the pair of first MOS transistors, and a second gate threshold voltage that is higher than the first gate threshold voltage is set to the pair of second MOS transistors.

7. An operational amplifier according to claim 2, wherein a first gate threshold

voltage is set to the pair of first MOS transistors and the third MOS transistor respectively, and a second gate threshold voltage that is higher than the first gate threshold voltage is set to the pair of second MOS transistors and the fourth MOS transistor respectively.